INTEGRATED CIRCUIT MEMORY DEVICES PROVIDING PER-BIT REDUNDANCY AND METHODS OF OPERATING SAME

ABSTRACT OF THE DISCLOSURE

An integrated circuit memory device includes a plurality of memory cells arranged as a plurality of blocks. Each of the blocks includes a plurality of primary memory cells that are coupled and decoupled to and from respective input/output lines responsive to a primary column select line and a plurality of redundant memory cells that are coupled and decoupled to and from respective ones of the input/output lines responsive to a redundant column select line. The device further includes a column select circuit, coupled to the primary column select lines and to the redundant column select lines, that drives a first primary column select line responsive to application of a first column address input and that drives a first redundant column select line in place of the first primary column select line responsive to application of a second column address input. The device also includes a plurality of sense amplifiers and an input/output control circuit configurable to selectively connect input/output lines to a sense amplifier such that a primary memory cell associated with the first primary column select line is coupled to the sense amplifier responsive to the first column address input and such that a redundant memory cell associated with the first redundant column select line is coupled to the sense amplifier responsive to the second column address input. Related operating methods are also discussed.